V6300 Product Brief

Version: **0.8**
Release Date: **July 15, 2017**

Specifications are subject to change without notice.

© 2017 Vango Technologies, Inc.

This document contains information that is proprietary to Vango Technologies, Inc.

Unauthorized reproduction of this information in whole or in part is strictly prohibited.

General Description

The V6300 is a narrowband Power Line Communication (PLC) processor chip. The V6300 integrates one 32-bit MCU, one 32-bit DSP, one embedded Flash memory, two UART interfaces, one SPI Master controller, one SPI Slave interface, one I^2C Master interface, PLC MAC/PHY layer functions, and Analog Front-End (AFE). Accompanied with Vango's high-current drive line driver chip (V6000), the V6300 forms a complete modem solution to support all known narrowband PLC Standards.

Features

- Supporting multiple narrowband PLC Standards: G3-PLC, IEEE P1901.2, PRIME, ITU-T G.hnem; also supporting single-carrier or multi-carrier PLC with FSK or BPSK/DBPSK modulation schemes
- With high-linearity and high-current drive line driver (V6000) having integrated receive functions, it offers the lowest BOM cost for G3-PLC/PRIME standards.
- Supporting frequency bands: CENELEC, FCC, ARIB, and proprietary mode (up to 2MHz)
- Supporting modulations: Selectable differential and coherent BPSK, QPSK, 8PSK, and coherent 16QAM
- Supporting IPv6 networking layer
- Supporting G3-PLC compliant 6LoWPAN adaptation layer with optimized network formation and mesh routing function
- Supporting HW AES-128
- Two UART interfaces (UART0 and UART1). UART1 is high-speed UART supporting up to 500-Kbps baud rate.
- One SPI Master with two chip select pins. It can be used to control wireless transceiver, metering, or other SPI devices.
- One SPI Slave interface for alternative data interface with Master processor chip
- One I^2C Master interface to control other I^2C devices
- 256-KB embedded Flash memory
- Supporting In-System Programming (ISP) of Flash memory via UART0 or SPI Slave interface
- Up to 32 programmable GPIOs for maximal flexibility
- 3.3-V digital I/O. UART pins are 5 V tolerant.
- Integrated LDO (3.3 V to 1.2 V)
- Packages:
  - V6300N: 68-pin QFN
- Operating temperature: -40 °C ~ +85 °C

System Block Diagram

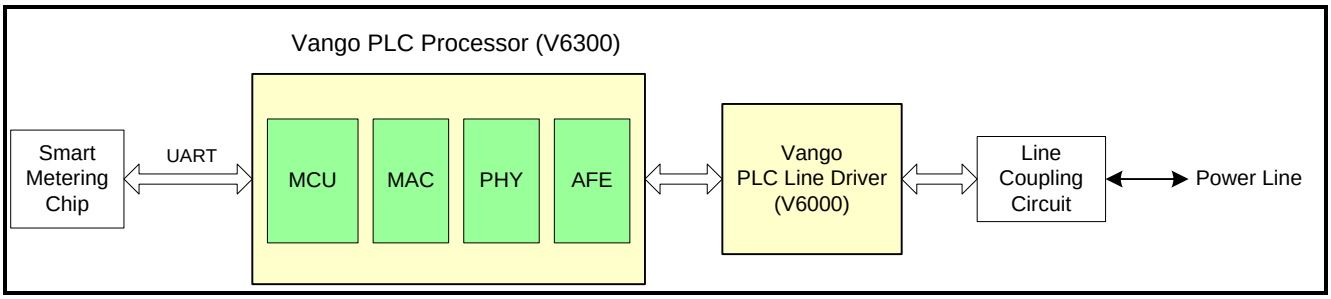


Figure 1. Example of Leaf Node Application

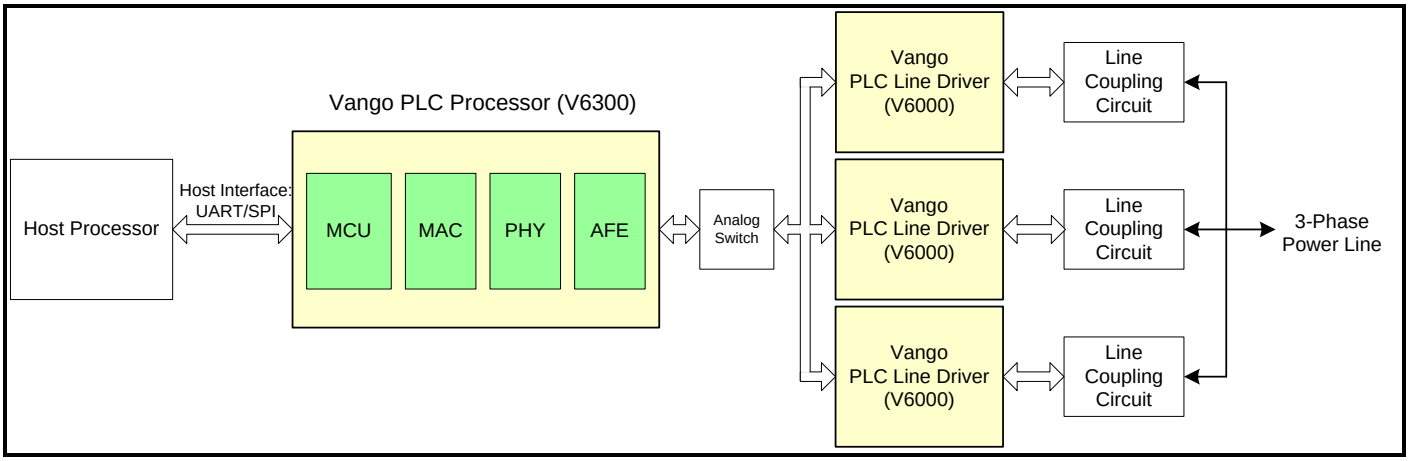
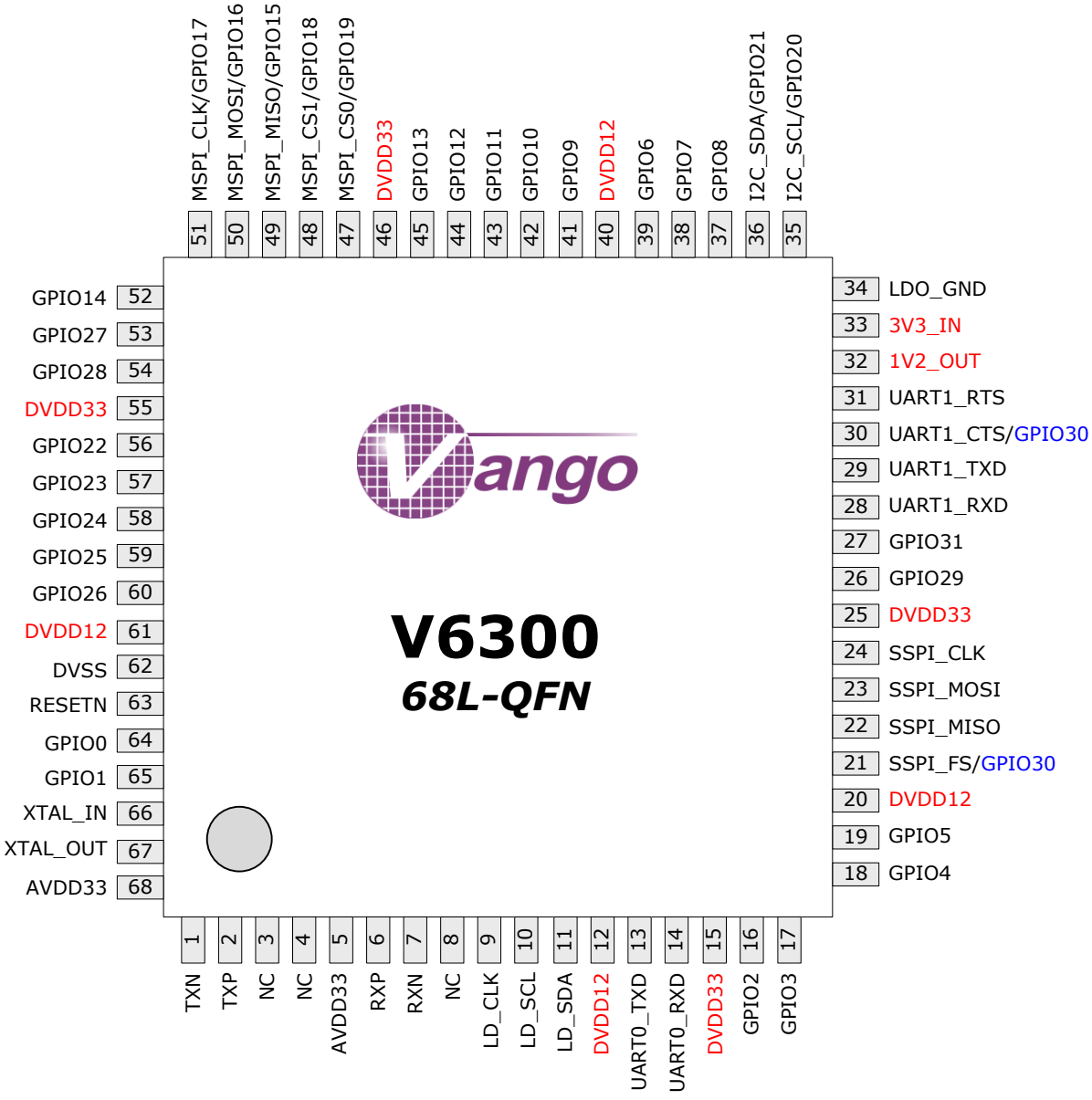


Figure 2. Example of Concentrator Application

Pin Assignments

68L-QFN



NOTE: The exposed thermal pad is connected to the ground.

Pin Descriptions

68L-QFN

(Pin type: "O"=Output, "I"= Input, "P"=Power, "G"=Ground)

No.	Mnemonic	Type	Description
1	TXN	O	DAC differential output (Negative) to line driver chip (V6000)
2	TXP	O	DAC differential output (Positive) to line driver chip (V6000)
3	NC		NC. Always keep floating
4	NC		NC. Always keep floating
5	AVDD33	P	Analog 3.3-V power
6	RXP	I	ADC differential input (Positive) from line driver chip (V6000)
7	RXN	I	ADC differential input (Negative) from line driver chip (V6000)
8	NC		NC
9	LD_CLK	O	Clock output to line driver chip (V6000)
10	LD_SCL	O	Line driver (V6000) control interface clock output
11	LD_SDA	I/O	Line driver (V6000) control interface data
12	DVDD12	P	Digital 1.2-V power
13	UART0_TXD	O	Low-Speed UART port 0: Data output Supporting baud rate from 1200 bps to 115200 bps
14	UART0_RXD	I	Low-Speed UART port0: Data input Supporting baud rate from 1200 bps to 115200 bps
15	DVDD33	P	Digital 3.3-V power
16	GPIO2	I/O	General Purpose I/O
17	GPIO3	I/O	General Purpose I/O
18	GPIO4	I/O	General Purpose I/O
19	GPIO5	I/O	General Purpose I/O
20	DVDD12	P	Digital 1.2-V power

No.	Mnemonic	Type	Description
21	SSPI_FS GPIO30	I I/O	Slave SPI frame sync input General Purpose I/O GPIO30 can be used either on pin 21 or pin 30.
22	SSPI_MISO	O	Slave SPI data output
23	SSPI_MOSI	I	Slave SPI data input
24	SSPI_CLK	I	Slave SPI clock input
25	DVDD33	P	Digital 3.3-V power
26	GPIO29	I/O	General Purpose I/O
27	GPIO31	I/O	General Purpose I/O
28	UART1_RXD	I	High-speed UART port 1: Data input Supporting baud rate from 1200 bps to 500K bps
29	UART1_TXD	O	High-speed UART port 1: Data output Supporting baud rate from 1200 bps to 500K bps
30	UART1_CTS GPIO30	O I/O	High-speed UART port 1: Clear to Send General Purpose I/O GPIO30 can be used either on pin 21 or pin 30.
31	UART1_RTS	I	High-speed UART port 1: Request to Send
32	1V2_OUT	P	Internal LDO 1.2-V output It must be tied to all the 1.2-V power pin of V6300
33	3V3_IN	P	Internal LDO 3.3-V input
34	LDO_GND	G	Internal LDO ground
35	I2C_SCL GPIO20	O I/O	Master I^2C port serial clock General Purpose I/O
36	I2C_SDA GPIO21	I/O I/O	Master I^2C port serial data General Purpose I/O
37	GPIO8	I/O	General Purpose I/O
38	GPIO7	I/O	General Purpose I/O

No.	Mnemonic	Type	Description
39	GPIO6	I/O	General Purpose I/O
40	DVDD12	P	Digital 1.2-V power
41	GPIO9	I/O	General Purpose I/O
42	GPIO10	I/O	General Purpose I/O
43	GPIO11	I/O	General Purpose I/O
44	GPIO12	I/O	General Purpose I/O
45	GPIO13	I/O	General Purpose I/O
46	DVDD33	P	Digital 3.3-V power
47	MSPI_CS0 GPIO19	O I/O	Master SPI select 0 General Purpose I/O
48	MSPI_CS1 GPIO18	O I/O	Master SPI select 1 General Purpose I/O
49	MSPI_MISO GPIO15	I I/O	Master SPI data input General Purpose I/O
50	MSPI_MOSI GPIO16	O I/O	Master SPI data output General Purpose I/O
51	MSPI_CLK GPIO17	O I/O	Master SPI clock output General Purpose I/O
52	GPIO14	I/O	General Purpose I/O
53	GPIO27	I/O	General Purpose I/O
54	GPIO28	I/O	General Purpose I/O
55	DVDD33	P	Digital 3.3-V power
56	GPIO22	I/O	General Purpose I/O
57	GPIO23	I/O	General Purpose I/O
58	GPIO24	I/O	General Purpose I/O
59	GPIO25	I/O	General Purpose I/O
60	GPIO26	I/O	General Purpose I/O

No.	Mnemonic	Type	Description
61	DVDD12	P	Digital 1.2-V power
62	DVSS	G	Must be tied to GND
63	RESETN	I	Reset input (Active low). It should be pulled low at least 100 ms for reset period.
64	GPIO0	I/O	General Purpose I/O
65	GPIO1	I/O	General Purpose I/O
66	XTAL_IN	I	Input of crystal oscillator driver (24 MHz)
67	XTAL_OUT	O	Output of crystal oscillator driver
68	AVDD33	P	Analog 3.3-V power