LATCH UP TEST REPORT

Company ：**Vango Technologies, Inc.**

Address ：**F/9, Haiyue Building, 788 Danfeng Rd, Binjiang District, Hangzhou, Zhejiang, P.R.China, 310051**

Model Name ：**V9811A**

Date Received ：November 11, 2016

Date Tested ：November 11, 2016

TESTING LABORATORY IS ACCREDITED BY:

IEC/IECQ 17025 certificate of independent test laboratory approval

CB Certificate No.: 1.72.0031/B IECQ Certificate No.: IECQ-L NSAIUS 09.0005

ISO 9001 certificate is approved by TUV CERT certification body of TUV NORD Cert GmbH

WE HEREBY CERTIFY THAT:

The test(s) shown in the attachment were conducted according to the indicating procedures. We assume full responsibility for the accuracy and completeness of these tests and vouch for the qualifications of all personnel performing them.

	Name	Signature	Date
Testing Engineer	Jian shen	Jian shen	2016/11/11
Approving Manager	Jianbo Song	Jianbo Song	2016/11/11

Note：

1. This report will be invalid if reproduced in whole or in part.
2. This report refers only to the specimen(s) submitted to test, and is invalid if used separately.
3. This report is ONLY valid with the examination seal and signature of this institute.
4. The tested specimen(s) will only be preserved for thirty days from the date issued, if not collected by the applicant.
5. The failure criteria of all ESD tests should be based on the result of parametric and functional testing conducted by the customer, which follows the statement of international standards. Thus, the judgment of the curve traces provided in this report is for reference ONLY.

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1. GENERAL INFORMATION

1.1 DESCRIPTION OF UNIT

MANUFACTURER	：Vango Technologies, Inc.
DEVICE NAME	：V9811A
PACKAGED / PIN COUNT	：QFP64
REFERENCE DOCUMENT	：JEDEC STANDARD NO.78D NOVEMBER 2011
TRIGGER CURRENT	：50mA (±) ~200mA (±) Step:50mA (±)
V SUPPLY OVER VOLTAGE TEST	：3.25V~5.25V(+) , Step: 1.0V(+) ：2.0V~3.0V(+) , Step: 1.0V(+)
PULSE DURATION	：10 ms
TEST TEMPERATURE	：ROOM TEMPERATURE
SAMPLE QUANTITY	：9 pcs
FAILURE CRITERIA	：If absolute Inom is < 25 mA, then absolute Inom + 10mA is used; Or If absolute Inom is > 25 mA, then > 1.4X absolute Inom is used;

2. LATCH UP TEST

2.1 TEST EQUIPMENT

Test Equipment	Equipment S/N	Calibration Date:	Recommended Due Date:
KEYTEK ZAPMASTER MK2 768	1603181	April 19, 2016	April 18, 2017

2.2 LABORATORY AMBIENCE CONDITION

Temperature：23±5°C

Relative humidity：55%±10% (RH)

2.3 REFERENCE DOCUMENT

The test is based on JEDEC STANDARD NO.78D NOVEMBER 2011

2.4 TEST CONDITION

I Trigger

Over Voltage Test

2.5 SUMMARY OF TEST

Trigger Mode	Test Pin	Sample Quantity	Tested Result	V or I Limits	I Trigger : Class Ⅰ
I Trigger (+)	I/P3.3V	3	PASS +200mA	+5.4V	**Temperature Classification:** CLASS Ⅰ: For Latch-up test at room temperature CLASS Ⅱ: For Latch-up test at maximum-rate ambient temperature
	O/P3.3V		PASS +200mA	+5.4V	
	I/O3.3V		PASS +200mA	+5.4V	
I Trigger (-)	I/P3.3V	3	PASS -200mA	-1.8V	
	O/P3.3V		PASS -200mA	-1.8V	
	I/O3.3V		PASS -200mA	-1.8V	
Over Volt Test V_{supply}	VCC3.3V	3	PASS +5.25V	+600mA	
	VCC2.0V		PASS +3.0V	+600mA	

Group	Pins
I/P3.3V	2,3, 4,10-16,63,64
O/P3.3V	1
I/O3.3V	7,9,17-62
VCC2.0V	5
VCC3.3V	6
VSS	8,42

2.6 CONTENTS OF TEST

I Trigger (Positive)			
Tested Pin	Sample No. & Failed current (mA)		
	#L1	#L2	#L3
2	PASS+200mA	PASS+200mA	PASS+200mA
3	PASS+200mA	PASS+200mA	PASS+200mA
10	PASS+200mA	PASS+200mA	PASS+200mA
11	PASS+200mA	PASS+200mA	PASS+200mA
12	PASS+200mA	PASS+200mA	PASS+200mA
13	PASS+200mA	PASS+200mA	PASS+200mA
14	PASS+200mA	PASS+200mA	PASS+200mA
15	PASS+200mA	PASS+200mA	PASS+200mA
16	PASS+200mA	PASS+200mA	PASS+200mA
63	PASS+200mA	PASS+200mA	PASS+200mA
64	PASS+200mA	PASS+200mA	PASS+200mA
4	PASS+200mA	PASS+200mA	PASS+200mA
1	PASS+200mA	PASS+200mA	PASS+200mA
5	PASS+200mA	PASS+200mA	PASS+200mA
6	PASS+200mA	PASS+200mA	PASS+200mA
9	PASS+200mA	PASS+200mA	PASS+200mA
17	PASS+200mA	PASS+200mA	PASS+200mA
18	PASS+200mA	PASS+200mA	PASS+200mA
19	PASS+200mA	PASS+200mA	PASS+200mA
20	PASS+200mA	PASS+200mA	PASS+200mA
21	PASS+200mA	PASS+200mA	PASS+200mA
22	PASS+200mA	PASS+200mA	PASS+200mA
23	PASS+200mA	PASS+200mA	PASS+200mA
24	PASS+200mA	PASS+200mA	PASS+200mA
25	PASS+200mA	PASS+200mA	PASS+200mA
26	PASS+200mA	PASS+200mA	PASS+200mA
27	PASS+200mA	PASS+200mA	PASS+200mA
28	PASS+200mA	PASS+200mA	PASS+200mA
29	PASS+200mA	PASS+200mA	PASS+200mA
30	PASS+200mA	PASS+200mA	PASS+200mA
31	PASS+200mA	PASS+200mA	PASS+200mA
32	PASS+200mA	PASS+200mA	PASS+200mA
33	PASS+200mA	PASS+200mA	PASS+200mA
34	PASS+200mA	PASS+200mA	PASS+200mA
35	PASS+200mA	PASS+200mA	PASS+200mA
36	PASS+200mA	PASS+200mA	PASS+200mA
37	PASS+200mA	PASS+200mA	PASS+200mA
38	PASS+200mA	PASS+200mA	PASS+200mA
39	PASS+200mA	PASS+200mA	PASS+200mA
40	PASS+200mA	PASS+200mA	PASS+200mA
41	PASS+200mA	PASS+200mA	PASS+200mA

42	PASS+200mA	PASS+200mA	PASS+200mA
43	PASS+200mA	PASS+200mA	PASS+200mA
44	PASS+200mA	PASS+200mA	PASS+200mA
45	PASS+200mA	PASS+200mA	PASS+200mA
46	PASS+200mA	PASS+200mA	PASS+200mA
47	PASS+200mA	PASS+200mA	PASS+200mA
48	PASS+200mA	PASS+200mA	PASS+200mA
49	PASS+200mA	PASS+200mA	PASS+200mA
50	PASS+200mA	PASS+200mA	PASS+200mA
51	PASS+200mA	PASS+200mA	PASS+200mA
52	PASS+200mA	PASS+200mA	PASS+200mA
53	PASS+200mA	PASS+200mA	PASS+200mA
54	PASS+200mA	PASS+200mA	PASS+200mA
55	PASS+200mA	PASS+200mA	PASS+200mA
56	PASS+200mA	PASS+200mA	PASS+200mA
57	PASS+200mA	PASS+200mA	PASS+200mA
58	PASS+200mA	PASS+200mA	PASS+200mA
59	PASS+200mA	PASS+200mA	PASS+200mA
60	PASS+200mA	PASS+200mA	PASS+200mA
61	PASS+200mA	PASS+200mA	PASS+200mA
7	PASS+200mA	PASS+200mA	PASS+200mA
62	PASS+200mA	PASS+200mA	PASS+200mA

I Trigger (Negative)			
Tested Pin	Sample No. & Failed current (mA)		
	#L4	#L5	#L6
2	PASS-200mA	PASS-200mA	PASS-200mA
3	PASS-200mA	PASS-200mA	PASS-200mA
10	PASS-200mA	PASS-200mA	PASS-200mA
11	PASS-200mA	PASS-200mA	PASS-200mA
12	PASS-200mA	PASS-200mA	PASS-200mA
13	PASS-200mA	PASS-200mA	PASS-200mA
14	PASS-200mA	PASS-200mA	PASS-200mA
15	PASS-200mA	PASS-200mA	PASS-200mA
16	PASS-200mA	PASS-200mA	PASS-200mA
63	PASS-200mA	PASS-200mA	PASS-200mA
64	PASS-200mA	PASS-200mA	PASS-200mA
4	PASS-200mA	PASS-200mA	PASS-200mA
1	PASS-200mA	PASS-200mA	PASS-200mA
5	PASS-200mA	PASS-200mA	PASS-200mA
6	PASS-200mA	PASS-200mA	PASS-200mA
9	PASS-200mA	PASS-200mA	PASS-200mA
17	PASS-200mA	PASS-200mA	PASS-200mA
18	PASS-200mA	PASS-200mA	PASS-200mA
19	PASS-200mA	PASS-200mA	PASS-200mA
20	PASS-200mA	PASS-200mA	PASS-200mA
21	PASS-200mA	PASS-200mA	PASS-200mA
22	PASS-200mA	PASS-200mA	PASS-200mA
23	PASS-200mA	PASS-200mA	PASS-200mA
24	PASS-200mA	PASS-200mA	PASS-200mA
25	PASS-200mA	PASS-200mA	PASS-200mA
26	PASS-200mA	PASS-200mA	PASS-200mA
27	PASS-200mA	PASS-200mA	PASS-200mA
28	PASS-200mA	PASS-200mA	PASS-200mA
29	PASS-200mA	PASS-200mA	PASS-200mA
30	PASS-200mA	PASS-200mA	PASS-200mA
31	PASS-200mA	PASS-200mA	PASS-200mA
32	PASS-200mA	PASS-200mA	PASS-200mA
33	PASS-200mA	PASS-200mA	PASS-200mA
34	PASS-200mA	PASS-200mA	PASS-200mA
35	PASS-200mA	PASS-200mA	PASS-200mA
36	PASS-200mA	PASS-200mA	PASS-200mA
37	PASS-200mA	PASS-200mA	PASS-200mA
38	PASS-200mA	PASS-200mA	PASS-200mA
39	PASS-200mA	PASS-200mA	PASS-200mA
40	PASS-200mA	PASS-200mA	PASS-200mA
41	PASS-200mA	PASS-200mA	PASS-200mA
42	PASS-200mA	PASS-200mA	PASS-200mA

43	PASS-200mA	PASS-200mA	PASS-200mA
44	PASS-200mA	PASS-200mA	PASS-200mA
45	PASS-200mA	PASS-200mA	PASS-200mA
46	PASS-200mA	PASS-200mA	PASS-200mA
47	PASS-200mA	PASS-200mA	PASS-200mA
48	PASS-200mA	PASS-200mA	PASS-200mA
49	PASS-200mA	PASS-200mA	PASS-200mA
50	PASS-200mA	PASS-200mA	PASS-200mA
51	PASS-200mA	PASS-200mA	PASS-200mA
52	PASS-200mA	PASS-200mA	PASS-200mA
53	PASS-200mA	PASS-200mA	PASS-200mA
54	PASS-200mA	PASS-200mA	PASS-200mA
55	PASS-200mA	PASS-200mA	PASS-200mA
56	PASS-200mA	PASS-200mA	PASS-200mA
57	PASS-200mA	PASS-200mA	PASS-200mA
58	PASS-200mA	PASS-200mA	PASS-200mA
59	PASS-200mA	PASS-200mA	PASS-200mA
60	PASS-200mA	PASS-200mA	PASS-200mA
61	PASS-200mA	PASS-200mA	PASS-200mA
7	PASS-200mA	PASS-200mA	PASS-200mA
62	PASS-200mA	PASS-200mA	PASS-200mA

Over Voltage Test for V_{supply}			
Tested Pin	Sample No. & Failed Volt (V)		
	#L7	#L8	#L9
5	PASS	PASS	PASS
6	PASS	PASS	PASS